

QS7X00

Flexible networking solutions designed for Service Providers from Access, Aggregation to Core networks

Key Features

- Flexible networking solution, designed for Service Providers from Access, Aggregation to Core networks
- High-speed integrated single-chip switching and routing device
- 10 GbE, 25 GbE, 40 GbE, 100 GbE, and 400 GbE interfaces
- Universal PAM4 56G serdes for network and fabric interfaces
- Scalable hierarchical traffic manager, with deep packet buffer
- Hardware support for IEEE 1588v2 implementation with precise time stamping
- Large on-chip lookup tables with dynamic resource allocation.

Supported applications

- Carrier-grade core and aggregation IP/MPLS routers
- Data center leaf, spine, and DCI switches
- High-capacity deep-buffering ToR and Border switches for data center.

Overview

The QS7x00 is a multifunctional network packet processor, enabling high capacity and feature rich routing and switching platforms for modern enterprise, datacenter and service provides networks. The QS7x00 is operating at Layer 2 through Layer 4 and supporting up to 16 x 400 GbE ports, 32×100 GbE ports, 128×25 GbE/10 GbE ports or mixed 10/25/100/400 GbE configurations.

The QS7x00 can be used to build a scalable product line based on a unified architecture that addresses many capacity and functional capabilities required for the following applications:

- High speed spine and ToR switches with deep buffering and HQoS capabilities for modern cloud datacenter deployments
- Multi-terabit core and edge routers for carrier network applications
- Modular and fixed chassis for enterprise networks

The versatile traffic manager integrates deep-packet buffers with a hierarchical scheduling scheme that allows carrier-class quality-of-service (QoS) feature set, including granular per-customer and perservice scheduling, as well as tunneling and overlay networks. The flexible packet pipeline provides rich functionality, dynamic hardware resource allocation for different use cases, and support for future-oriented protocols and technologies.

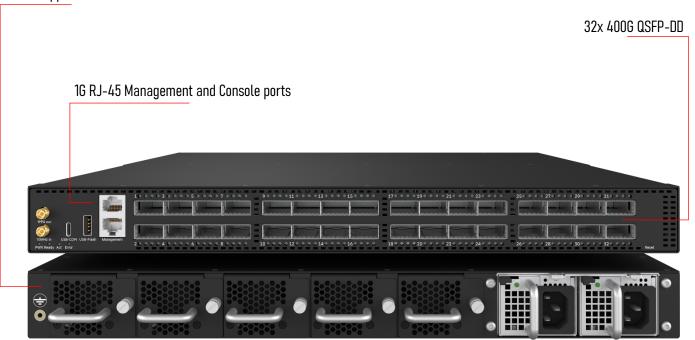


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Features

- Incorporates 400GbE switch silicon
- Quad Core Risc-V CPU, Hardware Root of Trust (ROT)
- High-performance 6.4 Tbps full-duplex routing and switching
- 128 universal PAM4 56G SerDes for network and fabric interfaces
- Flexible network interface:
 - 10 GbE, 25 GbE, 40 GbE, 100 GbE, and 400 GbE interfaces
- Traffic manager
 - 4 GB external 2xGDDR6 DRAM packet buffer
 - Carrier-grade traffic manager
 - Hierarchical traffic shaping and policing
 - Dynamic packet memory allocation
- Flexible and programmable packet processor
 - Multilayer switching and routing
 - MPLS and Segment Routing support
 - L2VPN, VPLS, EVPN, L3VPS services
 - Tunneling encapsulations, including GRE and VXLAN
 - Large on-chip lookup table for massive Internet scale
 - Flexible resource allocation for different applications
 - Extensive OAM and Telemetry support
- PTP IEEE 1588v2 with precise hardware based time stamping



• Physical parameters

- Dimensions (WxDxH): 438.4 mm x 648.2 mm x 44 mm
- Weight: 14.53 kg (32.03 lb)

Cooling

- Front-to-back airflow (0°C 40°C)
- Fans: Hot-swappable 4 + 1 redundant fans

• Operating

- Operating Temperature: 0°C to 40°C (32°F to 104°F)
- Storage Temperature: -40°C to 70°C (-40°F to 158°F)
- Operating Humidity: 5% to 85% (RH), noncondensing

Regulatory Compliance

- EMI (CE Mark, EN55032 Class A EN55024/35, EN 301 489-1, EN 301 489-19, EN 303413, FCC Part 15 Subpart B Class A EN 300 386)
- Safety (UL 62368-1 Ed.3, IEC/EN 60950-1, IEC/EN 62368-1 Ed.3, UL 60960)
- Environmental Compliance: (Storage: ETSI 300 019-2-1 Class T1.2, Transportation: ETSI 300 019-2-2 Class T2.3, Vibration: ETS EN 300 019-2-3 Class 3.2/ IEC 60068-2-64, Operating Bump Test: ETS EN 300 019-2-3 Class 3.2/ IEC60068-2-27, Acoustic Noise: ETS 300753, RoHS-6 Compliant)